module alu\_tb;

reg [7:0] A, B ;

reg [3:0] ALU\_Sel;

wire [8:0] ALU\_Result;

alu a1(A, B, ALU\_Sel, ALU\_Result);

initial

begin

ALU\_Sel=4'b0000;//add

A=8'b11111111; B=8'b00000000; // A = 0, B = 0

#50 A=8'b1111\_0000; B=8'b0000\_1111; // A = 240, B = 15

#50 A=8'b1111\_1111; B=8'b1111\_1111; // A = 255, B = 255

#50;

end

initial

$monitor ($time , " A=%d, B=%d, ALU\_Opcode=%d, ALU\_Result=%d", A, B, ALU\_Sel, ALU\_Result);

initial begin

$dumpfile("dump.vcd"); $dumpvars;

end

endmodule